REMARKS

In the Office Action mailed 23 December 2003, claims 1-17 and 29-36 were rejected, while claims 18-28 were allowed. Claims 11 and 29-32 were rejected under 35 U.S.C. §112, second paragraph, as allegedly indefinite, while claims 1-17 and 29-36 were rejected under 35 U.S.C. §103(a) based various combinations of references rooted around a base combination of U.S. Patent No. 6,243,098 to Lauer et al. (the "Lauer et al. Patent") and U.S. Patent No. 5,163,095 to Kosaka (the "Kosaka Patent").

By this response, Applicant has amended claims 11 and 29-32 to change the language specified by the Examiner, and accordingly, to moot any problems under 35 U.S.C. §112, second paragraph. As these claim amendments should be self-explanatory, Applicant will not discuss them herein further except to submit that the rejection for indefiniteness should now be withdrawn.

Applicant has also amended paragraphs 22 and 26 of the specification to correct minor grammatical errors; no new matter is presented. More particularly, the quoted term "raypoint" in paragraph 22, line 6 of the original specification should clearly be plural ("raypoints"), and the words "may" and "set" of paragraph 26, line 4 of the original specification are clearly interposed; Applicant submits that the amendments to fix these inconsistencies are proper and should be permitted.

With respect to the rejections under 35 U.S.C. §103(a), Applicant submits that the outstanding rejection is improper - neither the Lauer et al. Patent nor the Kosaka Patent show the teachings of the present invention, and one skilled in the art would not have been led to or even looked at the Kosaka Patent (unless that person was addressing some specific purpose cellular biology device irrelevant to the present application). Because all rejections under 35 U.S.C. §103(a) are predicated upon this combination of references, all such rejections are improper and should be withdrawn for this reason alone. Applicant note that each one of the Examiner's rejections under 35 U.S.C. §103(a) seem to be founded upon an impermissible hindsight approach that clearly fails to meet the PTO's prima *facie* burden; the Examiner argues that each cited reference shows one or more features of the present invention, but there no prior art teaching at all that would have led anyone to make any combination of references as called for by the Examiner. For example, the only reason that

the Examiner has even looked for a reference relating to cache design (the Luick Patent) is because some of Applicant's claims use that term; there is no art of record that (a) identifies, confronts or in any way identifies a solution to Applicant's problem, (b) identifies anything analogous to Applicant's claim limitations relating to use of a spread memory layout, and a pagination structure that always results in image data being put into a predetermined sub-part of cache, and (c) a image data load structure that prevents unintended cache discard of image processing parameters. The Examiner's approach of responding to Applicant's claims by looking for and selecting individual references, including a raycasting patent, an oct-tree addressing patent, a biological cell imaging patent that mentions the term "page" (out of context), and an internet packet processing patent (without any statement in the art suggesting these combinations) and then concluding without further evidence that (any) combination of their elements would be "obvious" simply does not comport with the legally appropriate criteria for measuring obviousness at the time of invention. Applicant respectfully submits that no cited art shows Applicant's limitations, provides any approach to Applicant's problem, or discloses (implicitly or otherwise) any structure similar to Applicant's claimed solution. Applicant below further discusses why the individual claim rejections are improper, but it suffices to note here that the Examiner has clearly applied legally inappropriate criteria and that factually, the Examiner's conclusions are clearly erroneous.

Because any problem under 35 U.S.C. §112, second paragraph, has been mooted by amendment, and because the rejections under 35 U.S.C. §103(a) are improper, Applicant submits that the claims of the present application are allowable over the cited art, and Applicant respectfully prays for issuance of a notice of allowance.

I. The Present Invention, Revisited.

As explained by Applicant's specification, a problem has existed in the art relating to processing of voxels. Typically, such processing operates on large data sets and it is often difficult to perform real-time processing on non-special purpose machines. This difficulty may be tied to conventional usage of cache and other "quick access memory." Typically, both the data set and any processing parameters are stored in the main memory of the computer and extensive time is needed to continually fetch and return small portions of data and parameters. Most digital processors will have an on chip cache to avoid any delays and keep data "close to" the processor, but unfortunately, cache space is limited and is

generally managed in a manner that results in frequent replacement of needed parameters or data. When a subsequent "cache miss" occurs as the processor again looks for the needed data or parameters, an undesired time delay may be consumed in attempting to again retrieve the these data and parameters from main memory. See, e.g., page 2, paragraphs 5-6 of Applicant's specification.

To address these problems, Applicant's invention utilizes two techniques to ensure that processing parameters aren't overwritten in cache by frequent data calls[1] - The two techniques are (a) storing adjacent data together as a block, with forced data block size that is necessarily less than processor cache size, ideally less than cache size by an amount sufficient to account for simultaneous cache storage of all frequently-needed processing parameters, and (b) consistent data positioning within memory using a spread memory layout, so as to essentially (via page formatting) channel the loading of data and parameters always into mutually-exclusive portions of quick access memory in a consistent manner. By implementing these techniques, a processor can be assured of retention of needed processing parameters in cache while loading a new data block (typically a 8x8x8 voxel cube). This type of processing is especially useful in processing of volumetric data, for example, as a processor calculates and retains intermediate values for transparency, color, brightness and other raypoint while it loads a new cube of voxels into memory to calculate incremental raypoint values. A hypothetical page layout is illustrated in Applicant's FIG. 5, but the point is that the data is structured and stored in a manner such that loading of a page of new voxels from main memory does not result in unintended cache discard of needed processing parameters. This operation differs from conventional cache management techniques where, typically, cache contents are managed based primarily on frequency of use.

In the present rejection, Applicant's independent claims 1, 15 and 29 were rejected under 35 U.S.C. §103(a). Each of these claims (and necessarily, all of their dependent claims) recites limitations relating to these inventive features. For example,

[1] "Quick access memory" is defined at page 8 of Applicant's specification to be temporary memory used to store data periodically fetched from main memory. It could be on-chip cache (L1) or off-chip, (L2) cache, or some other transient memory used as a closer-than-main-memory source.

independent claim 1 requires a spread memory layout, defining multiple pages in memory, with portions of the data set mapped to a subset of each page, such that image data is mapped only into predetermined portions of quick access memory. Independent claim 15 speaks of means for mapping processing parameters to predetermined portions of cache, such that those parameters occupy different portions of cache than data, with addressing being such that processing parameters do not overwrite data and vice-versa. Rejected independent claim 29 speaks of sizing data subsets to occupy only a specific portion of each page in memory, and the paging being such that the data subsets when loaded into quick access memory such that the data subsets will occupy only specific memory portions of the quick access memory to thereby inhibit overwriting of processing parameters. As should be apparent from this description, Applicant's invention focuses on organization and formatting of data in (main) memory in a manner that "corresponds" to quick access memory (such as cache), and this approach is not suggested by the cited art (apart from the "blocking" technique called for by the Lauer et al. Patent, which is discussed further below).

Applicant will discuss the merits of the rejection below, but to foreshadow Applicant's remarks, neither the Lauer et al. Patent nor the Kosaka Patent (the keystone of all grounds of rejection advanced by the Examiner) relate to cache management. These patents do not deal with the same problem as Applicant faced (cache misses and associated delays) and they do not show or render obvious Applicant's claimed invention; the Examiner's other cited references do not bridge these shortcomings.

II. Legal Standard For Rejection Under 35 U.S.C. §103(a).

35 U.S.C. §103(a) provides for unpatentability "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

A rejection for obviousness is based on the underlying factual inquiries set forth in *Graham v. John Deere:* (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; (3) the level of ordinary skill in the art; and (4) objective evidence of secondary considerations. *Bausch & Lomb, Inc. v. Barnes-*

Hind/Hydrocurve, 796 F.2d 443, 447 (Fed. Cir. 1986). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. *In re Fritch, 972 F.2d 1260, 1266 (Fed. Cir. 1992).* The appropriate inquiry is *not* whether it would have been obvious to substitute an element, or modify the prior art, in a manner advanced by the Examiner, because that is not the appropriate test of patentability. *See, e.g., In re Fine, 837 F.2d 1071, 1075 (Fed. Cir. 1988).* Rather, to meet its burden of showing prima facie obviousness, the PTO must necessarily show some objective teaching that would lead one of ordinary skill to combine the relevant teachings to solve the problem confronting the applicant. *In re Fine, supra.*

III. Analysis Of The Rejection Of Claims Under 35 U.S.C. §103(a).

A. Rejection Of Claims 1-3, 9-10 and 12-14.

Claims 1-3, 9-10 and 12-14 were rejected over a combination of the Lauer et al. Patent and the Kosaka Patent; Applicant argues that this rejection is erroneous for several reasons. First, neither patent is addressed to the problem that confronted Applicant, and one or ordinary skill would therefore not have looked to these patents given the problems they address as likely to suggest an attack of Applicant's problem. Second, however, the combined teachings of these patents do not show any approach to Applicant's problem and they fail to disclose much of Applicant's claims.

The Lauer et al. Patent relates to a device that, in order to achieve real-time processing on laptops and desktops, uses DRAM and four techniques aimed at improving DRAM burst mode access - the four techniques include "blocking," "sectioning," "pin-reduction" and "mini-blocking." See, e.g., column 8, line 11 through column 9, line 31 of the Lauer et al. Patent. The only one of these techniques pertinent to the present invention is "blocking," which relates to a technique of organizing data in such a way that adjacent data is contained in adjacent memory addresses in a single module, by grouping data such that voxels of a block of size BxBxB (B equal to 4 or 8) are stored at consecutive memory addresses; data is skewed by block, with each block being stored in a different, adjacent memory module such that P adjacent processing pipelines can in parallel fetch P adjacent blocks, all concurrently and simultaneously. See, e.g., column 9, line 31 through column 10,

line 12 of the Lauer et al. Patent. Of the other three techniques taught as necessary by the Lauer et al. Patent, "sectioning" relates to dividing adjacent slices into P sections and by preserving the raypoints passing through these sections in an external storage module for processing purposes (see, e.g., column 10, line 13 through column 11, line 25 of the Lauer et al. Patent); "pin-reduction" relates to reducing the pin connections between parallel pipelines by B^2/B^3 (see, e.g., column 11, lines 26-59 of the Lauer et al. Patent); and finally, "mini-blocking" relates to utilization of only 2x2x2 blocks of voxels from the boundaries of adjacent sections instead of all voxels of each adjacent block. See, e.g., column 12, lines 8-22 of the Lauer et al. Patent.

The Kosaka Patent relates to a special purpose medical imaging device for isolating and viewing biological cells found within a planar sheath; it teaches that it is necessary to use a special architecture including a master CPU, multiple slave CPU boards, a specialized image data bus, and a separate control bus in order to detect and organize biological cells into different categories. This hardware is used to continually image the planar sheath and to detect, isolate, extract and save just small images centered about each detected cell (see, e.g., columns 1-2 of the Kosaka Patent); these small images are then categorized and used to build image files where each file contains multiple, similarly classified cells together as single images. The Kosaka Patent addresses two specific problems in field of these machines, namely, that a first machine type is required to isolate, extract, and transmit a cell image during a vertical blanking interval (which does not allow sufficient time), and that a second type of machine continually transmits image frame data as a video signal (with 60 interlaced frames per second) but "tells" each slave board when to listen to the bus to pick up image data for a particular cell (this second type suffers from the problem that image transmission for each cell can occur only every one-sixtieth of a second, and that master and slave CPUs are further burdened during with the need to handle memory logistics). See, e.g., column 4, lines 1-32 and column 6, line 55 through column 7, line 2, of the Kosaka Patent. To solve these problems, the Kosaka Patent teaches that it is necessary to use a slave memory board system having window setting and image editing subsystems (Col. 10, line 38 through Col. 11, line 2). The window setting system includes X and Y counters for offsets, a window setting memory and a timing circuit, while the editing memory is divided into pages according to class of cells, with each page being one image frame - see, e.g., FIGS. 8 and 9 - cells of a common type are grouped together and displayed as a unique

image frame, which is what the Kosaka Patent refers to by "pages." See, e.g., Col 10, line 64 through Col. 11, line 2. That is to say, "pages" in the Kosaka Patent do not refer to conventional memory pagination as that term would be used, but rather to different video files each dedicated to a class of biological cells. Image codes and page numbers (frame numbers) are used by the device proposed by the Kosaka Patent as enabling the real-time grouping and processing of cells in the special-purpose cell processing hardware referred to above, i.e., to overcome limitations in the prior art such as being required to work during the vertical blanking intervals of a video signal.

The Kosaka Patent in particular is related to special purpose cellular biology hardware and simply has nothing of relevance to the present invention - it apparently was relied upon in hindsight by the Examiner simply because the Examiner believes that mere mention of the word "page" in the Kosaka Patent would be useful in rejecting the present claims. Considering the differences between the present invention and the Lauer et al. Patent (either alone or combined with the Kosaka Patent), there is no justification for any position that one of ordinary skill would have viewed the invention of claims 1-3, 9-10 or 12-14 as obvious.[2]

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[2] Several irregularities exist in the Office Action that Applicant wishes to comment upon. First, in paragraphs 5 and 8, the Examiner incorrectly implies that the Kosaka Patent calls for mapping data to *predetermined* portions of a page. To the contrary, the Kosaka Patent calls for grouping biological cells by type and then assigning each cell to the next available position in a frame (each frame is a different category on cells) - otherwise stated, a newly detected cell is placed in a variable position in a frame depending based on already-discovered cells (See, e.g., FIG. 9 of the Kosaka Patent). This position is not "predetermined," i.e., it's the next available place. Second, in paragraphs 7 and 18 of the Office Action, the Examiner takes the position that the Lauer et al. Patent calls for pages to have a size that are the "minimum burst size of the cache." Applicant does not understand this usage, i.e., minimum burst size typically relates to how many memory lines one can access using a single instruction, not some inherent design feature of cache.

1. The Examiner Has Not Demonstrated Any Teaching Or Suggestion To Combine These References In Expectation Of Solving The Problem Applicant Confronted.

The primary problem faced by Applicant is delays caused by cache misses for needed processing parameters (as opposed to voxel data); to address this problem, Applicant's invention calls for a spread memory layout, with pages of specific size and format that effectively force group loading of image data always into a predetermined subset of cache, so as to deliberately put image data in a cache in a manner that will not cause unintended cache discard of processing parameters.

Viewed against this problem, the Lauer et al. Patent is directed to enabling real time raycasting on laptops and workstations, and it teaches that in order to solve this problem, one must use parallel processing and four specific processing techniques, including "blocking", "sectioning," "pin-reduction" and "mini-blocking". The approach of the Lauer et al. Patent is that these things are processing shortcuts that speed up processing; the Lauer et al. Patent does not address memory organization apart from stating that adjacent data should be stored in an adjacent manner (the so-called "blocking" technique of the Lauer et al. Patent.). As acknowledged by the Examiner, the Lauer et al. Patent does not show a spread memory layout and it also doesn't provide any teaching or suggestion as to how one can avoid or minimize cache discard of image processing parameters.

The Kosaka Patent relates to special purpose biological cell planar sheath imaging devices - there is no reason given in the record that would motivate someone to look at this patent as potentially providing a solution to Applicant's problem, or to somehow combine isolated elements of the Kosaka Patent with select elements of the Lauer et al. Patent. The Kosaka Patent has nothing to do with the technology of the Lauer et al. Patent, it does not mention inferentially or otherwise anything about the Lauer et al. Patent, it has little pertinence to raycasting or volume rendering, and it has no pertinence to the problem of how one might avoid cache misses while looking for image processing parameters; it specifically teaches that in order to overcome problems in planar sheath cell imaging and classifying devices, it is necessary to always use a master processor/multiple slave board system where separate image data and control busses are utilized. Quite simply, there exists no teaching or suggestion that would have motivated anyone at the time of invention to combine the Kosaka

Patent with the Lauer et al. Patent, and these references are clearly directed at different purposes and different problems that the problem faced by Applicant; if the Examiner believes that there is a teaching or suggestion in the prior art to combine these specific references, other than the claims at-issue, Applicant respectfully requests that the Examiner furnish documentary proof of a specific suggestion to make this combination.

2. <u>Differences Between The Rejected Claims And The Pertinent Art.</u>

Even taking the Kosaka and Lauer et al. Patents together, there are still substantial differences between that "aggregated art" and the claims at-issue. The Examiner's rejection of claims 1-3, 9-10 and 12-14 over the Lauer et al. and Kosaka Patents seems to be premised on the fact that the Lauer et al. Patent shows a form of data block interleaving, and that the Kosaka Patent merely mentions the word "page" (as explained above, this usage in the Kosaka Patent is taken out of context because, in the Kosaka Patent, it refers to different groups of frames - i.e., different video signals - but not to the conventionally-understood usage of the term as referring to consistently sized blocks of memory). Neither patent even deals with Applicant's problem of cache misses caused by processing parameter overwrite, and neither patent teaches that in order to solve this problem, one must use Applicant's specific solution of memory organization via page formatting so as to always write parameters and data into mutually exclusive parts of cache/quick access memory.

Applicant's claims 1-14 all depend from rejected independent claim 1, which reads as set forth below.

" 1. An apparatus comprising a data set stored on machine readable media, wherein:

the data set is divided into multiple subsets;

a spread memory layout is implemented on the machine-readable media, the spread memory layout defining multiple pages in memory, with a subset of data from the data set being mapped to one or more predetermined portions of each page, the portions being less than the capacity of each page; and

each page is sized to map to quick access memory of a processor, such that image data when fetched from the machine-readable media are mapped into one or more predetermined portions of quick access memory."

Applicant asserts that this claim (and all of claim set 1-14) contain substantial differences relative to the cited art; nothing in either referenced deals with the problem of minimizing cache misses caused through the discard of needed processing parameters, and nothing in either reference (a) deals with a cache management or management or a temporary "quick access memory" as used by the present invention, or (b) requires page formatting to correspond to cache size, and requiring data subsets to always fit within a predetermined portion of a page, so that when loaded, the data subsets will necessarily not cause discard of needed processing parameters. Nothing in either patent has any use of disclosure of a "spread memory" layout.

Applying the legal criteria for an obviousness determination, it is respectively submitted that nothing in the cited record suggests any approach to solving Applicant's problem. One faced with a problem of providing real-time rendering on a workstation or laptop might look to the Lauer et al. Patent, but would be instructed to use parallel processing and four specific techniques in order to achieve that end; they would be instructed to use this as opposed to Applicant's solution, and they would not be direct to use a solution involving page sizing to correspond to cache, a spread memory that deliberately leaves room for processing parameters and so forth. One faced with the problem of providing real-time rendering on a workstation or laptop would likely perceive no relevance at all in the Kosaka Patent - it relates to a special purpose cellular biology device, and the problem addressed by the Kosaka Patent (solving vertical blanking/master-slave coordination) simply would not lead one to "search through" that patent to hopefully find isolated concepts that could be applied to Applicant's problem. Indeed, the Kosaka Patent is cited by the Examiner simply because it uses the term "page" which it takes to mean separate video frames used to categorize biological cells in a planar sheath. Applicant concedes that pagination is one technique used in some memory management applications, but emphasize that the Kosaka Patent adds absolutely nothing to the cited art - it does not teach or suggest that memory "pagination" would be useful to solving a problem relating to cache misses caused by cache discard of processing parameters, it does not suggest (as the Examiner contends) that the

Lauer et al. Patent should be "modified" in any way, shape or form, and it does not suggest that one should effectively change the way that cache line discard occurs through the way that new image data is retrieved into cache and managed. Simply put, the differences between the cited art and the claims at issue are significant enough that the present rejection clearly cannot be maintained. Applicant therefore respectfully requests reconsideration of these claims.

B. <u>The Rejection Of Claims 4-8 And The Luick Patent.</u>

Claims 4-8 were rejected over a combination of the Lauer et al. Patent and the Kosaka Patent, in further view of U.S. Patent No. 6,473,835 to Luick (the "Luick Patent"). The Examiner cites the Luick Patent for the basic proposition that it would be obvious to use cache as a form of "quick access memory" but, otherwise, the Examiner relies upon the aforementioned rejection of claim 1; the essence of the Examiner's contention is that assuming that the Lauer et al. and Kosaka Patents represent the state of the art, it would be obvious to modify this art to apply to cache, and hence, Applicant's claims 4-8 should be considered unpatentable.

Applicant vigorously contests this approach as contrary to law, because what the Examiner has done in rejecting claims 4-8 has been to essentially assume that claim 1 to be prior art, and then suggest that claim 1 if combined with a new reference (the Luick Patent) would render claims 4-8 obvious. The impropriety of the Examiner's approach is especially clear when focusing on the Examiner's statement in paragraphs 16 and 17 "... it would have been obvious ... to modify Lauer and Kosaka to use cache as taught by Luick because it allows data to be accessed faster..." To the contrary, there is no statement or evidence anywhere that would lead one to "modify" the Lauer et al. or Kosaka Patents in any way, shape or form. If the Examiner believes to the contrary, then Applicant respectfully requests that the Examiner identify a documentary reference by column and line number where one skilled in the art is (a) specifically directed to look at any of the Lauer et al., Kosaka, and Luick Patents, and (b) specifically directed to discard all of the problems and teachings presented by those patents and instead apply specific elements selected by the Examiner from those patents to address Applicant's problem.

The Luick Patent relates to improvements in cache architecture in the abstract - it has no pertinence to volume rendering, image processing or to altering how cache line replacement occurs during special purpose applications. Rather, the Luick Patent relates to increasing the size of conventional L1 (i.e., on chip microprocessor cache) by implementing a n-way associative cache implemented in a n-1-way associative manner, with the "extra" column of data used as a transition look-aside buffer (TLB). The Luick Patent provides no teaching, suggestion, or clue that to avoid Applicant's problem, one should utilize a spread memory layout with pagination selected to force image data into a consistent subset of cache (not overlapping the portions of cache used for processing parameters). The Examiner has not demonstrated *any* teaching or suggestion that would lead one specifically to the Luick Patent, much less to discard *all* of the teachings of the Luick Patent (e.g., that one should necessarily build a *n*-way associative cache to operate as a *n-1* way associative cache) to somehow address "some" different problem that is not addressed by the Luick Patent. It is very apparent from the circumstances presented in this rejection that the only thing that has led to selection of the Luick Patent by the Examiner is that the Examiner, motivated by Applicant's claims, wants to find a documentary reference of the term "cache" someplace for the purpose of rejecting those claims.

The appropriate legal inquiry is *not* whether it would have been obvious to substitute an element, or modify the prior art, in a manner advanced by the Examiner, because that is not the appropriate test of patentability. *See, e.g., In re Fine, 837 F.2d 1071, 1075 (Fed. Cir. 1988).* Rather, to meet its burden of showing prima facie obviousness, the PTO must necessarily show some objective teaching that would lead one of ordinary skill to combine the relevant teachings to solve the problem confronting the applicant. *In re Fine, supra.* Applicant believes that it is very clear given the Examiner's "obvious to modify" approach that the Examiner has indeed applied the legally-erroneous standard.

Applicant respectfully submits that the rejection of claims 4-8 is in error and must be withdrawn, because there is no teaching or suggestion demonstrated in the record that would lead one to adopt memory management and cache management techniques as an approach to solving Applicant's problem. There is nothing in the record that would lead or motivate one to combine the Kosaka, Luick or Lauer et al. Patents, and even assuming arguendo, that one did make such a combination, nothing in this aggregated art shows or

suggests any solution to Applicant's problem, much less Applicant's claimed limitations. Withdrawal of the rejection of claims 4-8 is respectfully requested

C. **Rejection Of Claims 11, 15-16 and 29-36 And The Fiacco Patent.**

Claims 11, 29-32 and 35-36 were rejected over a combination of the Lauer et al. Patent and the Kosaka Patent, in further view of U.S. Patent No. 5,860,149 to Fiacco (the "Fiacco Patent"). Claims 15-16 and 33-34 were rejected over a further combination of these three patents with the Luck Patent.

The Fiacco Patent relates to the use of buffers to transmit data between a slower element and a faster one, so that the slow element is not overwhelmed and so that the faster element can perform other tasks; in particular, the Fiacco Patent relates to the problem of intermediate node header information creating inefficiencies in buffer-based processing of packets by imposing blocking problems for each packet in a message train. To address this problem, the Fiacco Patent proposes use of a single address for accessing multiple buffers, so that addition intermediate node header information has less of an impact (because a header imposes blocking problems only for the message train as a whole, rather than individually, for each packet in a message frame).

There is no disclosure, teaching, hint or anything else in the Fiacco Patent that has any application to the present invention - The Fiacco Patent does not relate to image processing, cache management, memory paging or anything else pertinent to the present invention.

The Examiner alludes to why he selected the Fiacco Patent in paragraphs 26, 28 and 34. In particular, the Examiner in paragraph 26 states that "Fiacco teaches that header buffers may be partitioned from payload data" that that "because buffers and data are in separate address locations, overwriting is inhibited." The Examiner apparently cites the Fiacco Patent for the proposition that in some applications control application and data may be separated - the Examiner's position is not readily understood beyond this, i.e., the Fiacco Patent deals with packet transmission - nothing is being "overwritten" anywhere in the Fiacco patent or the applicable technology. The problem the Fiacco Patent deals with is that packets typically are of fixed length, and that if lengthy header information is attached to each and every packet (e.g., to each one of 5 separate packets), then buffer storage becomes inefficient

because the header information is repeated - the Fiacco Patent proposes assigning header information and packets to different data blocks so that one address can be used to refer to header information and each of the 5 separate packets for example).

There is no teaching or suggestion in the Fiacco Patent of any application to Applicant's principle, and the Office Action again does not explain how or why one would look to the Fiacco Patent as providing anything likely to yield a solution to Applicant's problem. Again, Applicant believes that the Examiner has applied the legally impermissive approach to examination of using Applicant's claims themselves as a guide to selecting references showing isolated features in the prior art for the purposes of rejecting those claims - this is not the correct approach and should result in withdrawal of the rejection per se, *see, e.g., In re Fine, 837 F.2d 1071, 1075 (Fed. Cir. 1988).*[3] In this case, the Fiacco Patent shows partitioning a buffer into multiple parts to achieve efficiencies in terms of manipulating header information. There is no evidence in the record why someone of skill in the art at the time of invention would have been led to a buffer partitioning patent as providing any solution to Applicant's problem, and there is no evidence in the record why one would select the Fiacco and other specific patents (out of many thousands of patents that deal with buffers, caches, rendering, etc.) and make select combinations now advanced by the Examiner. The Fiacco Patent, and indeed, none of the cited art of record, teaches any approach to reducing or elimination overwrite of processing parameters caused by cache discard through manipulation of memory format, i.e., through pagination and a spread memory layout.

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[3] As stated by the Federal Circuit, "To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher. *W.L. Gore*, 721 F.2d at 1553, 220 USPQ at 312-13. It is essential that the decisionmaker forget what he or she has been taught at trial about the claimed invention and cast the mind back to the time the invention was made . . . to occupy the mind of one skilled in the art who is presented only with the references, and who is normally guided by the then-accepted wisdom in the art." *Id.* One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to depreciate the claimed invention."

It is respectively submitted that the outstanding rejection of claims 11, 15-16 and 29-36 is improper and must be withdrawn.

D. Rejection Of Claim 17 The Prevost et al. Patent.

The Examiner rejected claim 17 over a combination of the Lauer et al., Kosaka and Luick Patents, in further combination with U.S. Patent No. 5,123,084 to Prevost et al. (the "Prevost et al. Patent"). As explained at paragraph 38 of the Office Action, the Examiner cites the Prevost et al. Patent for the proposition that oct tree addressing is fast. According to the Examiner, because of this "teaching", any invention anywhere that uses oct-tree addressing must therefore be obvious, because doing so would improve performance. [The specific language used by the Examiner is that "therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lauer to use octree addressing as taught by Prevost because it is fast and will improve performance of the system."]

Again, Applicant disputes the Examiner and calls upon the Examiner to articulate where, by specific line number and column number, the Prevost et al. Patent *says* that one should modify the Lauer et al. Patent (or vice-versa, i.e., where by specific line number and column number the Lauer et al. Patent *says* that one should modify the Prevost et al. Patent) as likely to solve a problem neither of these references address. To the contrary, it is very clear hear that the Examiner has applied the wrong criteria for judging patentability, i.e., there has to be something that causes one skilled in the art to select specific references other than the claims at-issue, and there is absolutely no evidence in the art to support any of the Examiner's selections of art or the Examiner's conclusions relating to any "modification" of the individual references or their teachings.

In this case, the Prevost et al. Patent deals with the translation of 3D data that has been oct-tree encoded, so as to permit display from a target perspective and, with a specific architecture for this purpose; the Prevost et al. Patent does not have any teaching or suggestion applicable to solving Applicant's problem, and it does not suggest that data may be more efficiently processed via a spread memory layout function as called for by Applicant's claims. It is true that the Prevost et al. Patent does disclose the use of oct-tree encoding for volumetric data, but as stated by the Prevost et al. Patent, e.g., at column 1, lines

15-17, this is and has been well known in the art for some time. What the Prevost et al. Patent does not address, and what the Examiner does not address in the Office Action, is why one might specifically format memory in an oct-tree format so as to minimize cache misses of processing parameters... the Examiner's approach essentially conclusorily assumes this teaching and application, but this is why applicable law requires the demonstration of a roadmap in the prior art, i.e., the real essence of invention is the combining of engineering elements and structure to achieve new ends and solve problems, and it is the combination that the prior art has to show in order to be relevant to patentability, not simply show that individual elements of a claim have existed in isolation.

It is respectfully submitted that the Prevost et al. Patent adds nothing to the deficiencies in the Examiner's showing with respect to Applicant's other rejected claims - the Prevost et al. Patent was selected because it shows in isolation one element of some of Applicant's dependent claims, totally out of context of the present invention. There is absolutely no suggestion or teaching in the Prevost et al. Patent or anywhere else that suggests that one could or should use oct-tree addressing as a specific means to ensure that volume memory is organized so that a small cube (e.g., 8x8x8 voxel cube) can be loaded in isolation into a predetermined, consistent subset of cache, so as to enable retention of image processing parameters.

It is respectfully submitted that absent *any* evidence in the record of how one faced with Applicant's problem should approach solving that problem, the PTO cannot be said to have met its burden. The Examiner's conclusory statements to the contrary are not evidence, i.e., the Examiner needs to find and present *evidence* of a roadmap existing previously in the art for solving Applicant's problem, and that is not satisfied by simply identifying multiple references that show isolated, unrelated elements and then alleging without further evidence that it would have been obvious at the time of invention to combine those elements. Applicant respectfully submits that there is no such suggestion to combine the four references selected by the Examiner to reject claim 17, and that even given the aggregate teachings of those references, there still is no indication anywhere in the record of how one skilled in the art should go about solving Applicant's problem.

Reconsideration of the rejection of claim 17 is therefore respectfully requested.

IV. Conclusion.

Applicant submits that the rejection must be withdrawn, because there is no teaching or suggestion to combine references in the manner sought by the Examiner, and because such a showing is part of the Examiner's required burden in order to demonstrate a prima facie case of obviousness. Furthermore, the Examiner has not found even one reference that addresses the problem faced by Applicant or that teaches or suggest the principles of Applicant's claimed solution. Because the differences between the cited art and the claims under rejection are so dramatic, and because no cited reference sheds any light on any solution to Applicant's problem, it is respectfully submitted that one would not pick and choose isolated elements as the Examiner has done here, and that one of ordinary skill in the art would not view (in view of the references) Applicant's claimed solution as obvious given Applicant's problem - none of the cited references are pertinent to Applicant's problem, and even considered together, no combination of them shows or comes even close to the limitations of Applicant's claims.

Reconsideration of the outstanding rejection of claims is therefore respectfully requested.

Respectfully Submitted,

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CERTIFICATE OF MAILING (37 C.F.R. §1.8)
I hereby certify that this paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington D.C. 20231 on this 20 April 2004.

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Dated: 20 April 2004